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DISSERTATION INFORMATION

Research Title:	A Hybrid Asymmetric Pulse-Width-Modulation Strategy with Reduced Common-mode Voltage and Low Output Harmonic Distortion for a Three-Level Neutral-Point-Clamped Converter
Major:	Electrical Engineering
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MAIN CONTENTS AND CONTRIBUTIONS OF THE DISSERTATION

In three-level Neutral-Point-Clamped converters (3L-NPCs), high-frequency components of CMV due to large CMV magnitude have been known to induce bearing current in motors, thereby reducing the service lifetime of motors. In addition, the low-frequency components of CMV, specifically the third-order CMV component and its multiples, due to non-zero average CMV, have been attributed to difficulties in Common-mode (CM) filter design, heated CM inductors and low-frequency CM interference for sensitive equipment. Furthermore, reducing CMV magnitude gives rise to high output harmonic distortion. As a result, hardware- and software-based solutions have been proposed to mitigate the adverse effects of CMV. Nevertheless, hardware-based solutions have several drawbacks, such as an increase in the cost and volume of a system.

Meanwhile, the software-based ones, which only involve the modifications of pulse-width modulation (PWM) strategies, have distinct advantages, such as simplicity and low cost.

Therefore, based on the arguments mentioned earlier, this doctoral dissertation proposes an asymmetric hybrid PWM strategy, namely HRCMV-ASYM, for a three-level NPC converter to achieve reduced CMV magnitude, zero average CMV, and improved performance of harmonic distortion for the 3L-NPCs. To facilitate the description of HRCMV-ASYM, an in-depth analysis of the three-level zero-average-CMV space vector diagram and associated mathematical expressions are presented. Under the condition of zero average CMV, the three-level zero-average-CMV space vector diagram (3L-SVD) is divided into two distinct regions. Within which, zero-CMV vectors and virtual vectors are constructed. To pave the path for HRCMV-ASYM, two conventional zero-average-CMV PWM strategies, namely In-Phase Disposition Sinusoidal PWM (IPD-SPWM) without CMV magnitude reduction and Phase Opposition Disposition Sinusoidal PWM (POD-SPWM) with CMV magnitude reduction, are discussed to highlight the deficiencies in these two PWM schemes. Specifically, IPD-SPWM uses three nearest vectors at the expense of high CMV magnitude.

In comparison, POD-SPWM utilizes three nearest vectors and one distant vector in some regions, while it uses two nearest vectors and two distant vectors in others. Due to the two distant vectors, the harmonic distortion of POD-SPWM is significantly higher than that of IPD-SPWM. As a result, symmetric switching patterns, namely RCMV1, which are proposed, use three nearest vectors and one distant vector for all modulation regions to achieve lower harmonic distortion compared to POD-SPWM. Furthermore, a close inspection of the three-level zero-average-CMV space vector diagram reveals that it is feasible in some modulation regions to reduce further the harmonic distortion produced by RCMV1 by using the four nearest vectors. And this leads to asymmetric patterns (RCMV-ASYM). As the name implies, the asymmetric patterns (RCMV-ASYM) are designed asymmetrically to maintain the same six-per-carrier switchings as those of other schemes.

Owing to the four nearest vectors in RCMV-ASYM covering a portion of a modulation region, RCMV-ASYM is used in combination with RCMV1 to maintain low harmonic distortion, thereby leading to a hybrid asymmetric PWM strategy, namely HRCMV-ASYM. Simulation in MATLAB/Simulink and PLECS and experimental results for a 3L-NPC with the three-phase R-L load and three-phase induction motor again confirm that HRCMV-ASYM yields the lowest harmonic distortion as opposed to RCMV1 and POD-SPWM for a whole modulation range and different power factor conditions under the conditions of reduced CMV magnitude, zero average CMV, and comparable switching losses.

The main contributions of the doctoral dissertation are as follows:

1. The construction of the generalized three-level zero-average-CMV space vector diagram in terms of zero-CMV vectors and virtual vectors.
2. The comprehensive analysis of space vector characteristics of zero-average-CMV PWM strategies (ZACMV-PWMs) allows us to correctly predict the harmonic distortion of ZACMV-PWMs.
3. The two conventional ZACMV-PWMs, including POD-SPWM and IPD-SPWM, are analyzed from the virtual space vector perspective, thus revealing their drawbacks in terms of CMV reduction and harmonic distortion.
4. Based on these demerits of the two conventional ZACMV-PWMs, the new switching patterns, namely RCMV1, are proposed to reduce harmonic distortion while still achieving the same reduced CMV magnitude and zero average CMV as POD-SPWM.
5. An in-depth virtual space vector analysis of the three-level zero-average-CMV space vector diagram reveals that it is feasible to reduce further the harmonic distortion given by RCMV1

by making use of four nearest vectors instead of three nearest vectors and one distant vector in RCMV1, resulting in asymmetric switching patterns (RCMV-ASYM).

6. Owing to the four nearest vectors only covering a portion of the modulation subregion, a hybrid asymmetric PWM strategy, HRCMV-ASYM, is proposed. HRCMV-ASYM involves the use of RCMV1 and RCMV-ASYM.
7. In-depth simulation and experimental results conducted for a three-level NPC converter under the three-phase R-L load and a V/f three-phase induction motor confirm that HRCMV-ASYM produces the lowest harmonic distortion while still giving the same reduced CMV magnitude, zero average CMV, and comparable switching losses as RCMV1 and POD-SPWM.

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